

Reconciling nondeterminism and causality

Event structures for weak memory

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Reasoning on concurrent programs

Consider the program mp :

```
data = flag = 0
data := 17; || r ← flag;
flag := 1   || v ← data
```

Does $mp \models r = 1 \Rightarrow v = 17$?

Reasoning on concurrent programs

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Does `mp` $\models r = 1 \Rightarrow v = 17$?

Two main solutions to prove this:

- ▶ **Operational** semantics formalises the **machine**
- ▶ **Axiomatic** semantics formalises the **executions**

Operational semantics: machines as LTSs

Formalises an **abstract machine** running the program:

$$\langle (x := 1; t \parallel p) \odot \mu \rangle \xrightarrow{W_{x:=1}} \langle (t \parallel p) \odot \mu[x := 1] \rangle.$$

Transitions labelled by an action in $\Sigma ::= W_{x:=k} \mid R_{x=k} \mid \dots$

Executions of the program become **traces** of the LTS:

$$\langle mp \odot \mu \rangle \xrightarrow{W_{data:=17}} \xrightarrow{W_{flag:=1}} \xrightarrow{R_{flag=1}} \xrightarrow{R_{value=17}}$$

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- ⊕ Represents **nondeterministic branching points**.
↪ Liveness properties, whole program optimisations.
- ⊖ Combinatorial explosion due to **interleaving**.
↪ Hard to simulate, hard to reason on.

Axiomatic semantics

Formalises a program by the set of its valid **executions**:

program $\overset{\text{syntax}}{\rightsquigarrow}$ execution candidates $\overset{\text{model}}{\rightsquigarrow}$ executions
set of events+relations

Two candidates for mp:

W *data*:=17 R *flag*=0
po \downarrow \downarrow po
W *flag*:=1 R *data*=0

valid on all architectures

W *data*:=17 R *flag*=1
po \downarrow \downarrow po
W *flag*:=1 R *data*=0
 \nearrow rf

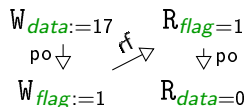
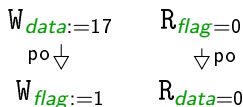
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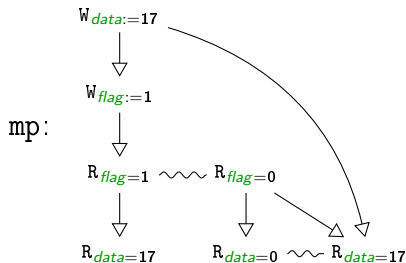
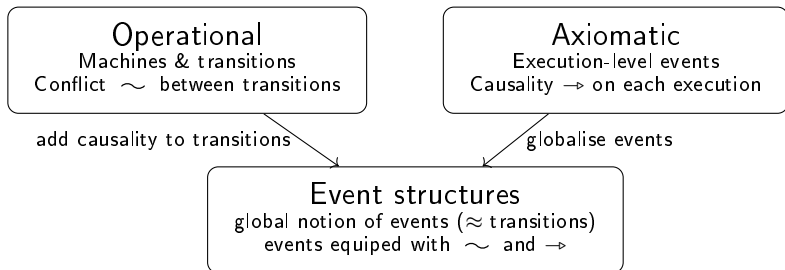


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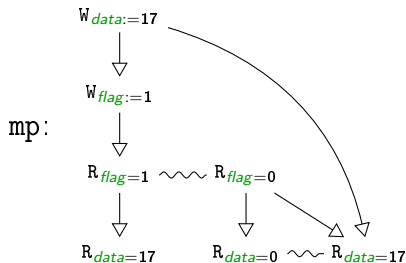
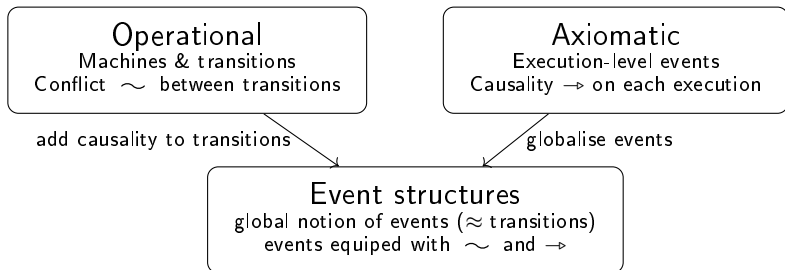
valid on some (eg. ARM)

- ⊕ **Causal** account of executions.
⇒ Easy to simulate; allows higher-level reasoning.
- ⊖ **Per-execution** modelling of the program.
⇒ No grip on the nondeterministic branching point

The best of both worlds: event structures



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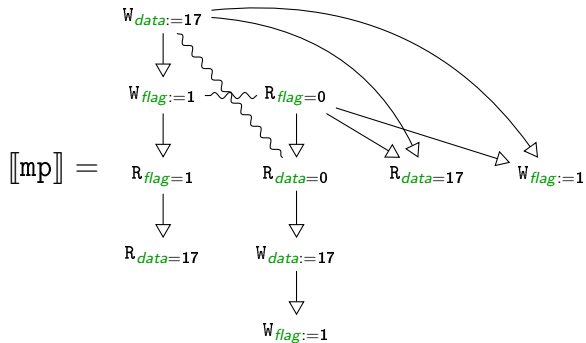


Maximal conflict-free subsets \leftrightarrow Axiomatic executions.

Outline of the talk

- (1) **From programs to event structures.**
The sequentially consistent case.
- (2) **A strong data-race-free theorem for TSO.**
Which preserves liveness properties.
- (3) **Relaxing coherence.**
Improving over the co of axiomatic semantics.
- (4) **Beyond assembly: higher-order languages**
When labels become moves.

I. FROM PROGRAMS TO EVENT STRUCTURES: NAIVE SC



Our language

We consider a simple imperative language:

$e ::= r \mid e + e \mid \dots$ **expressions**

$t ::= \epsilon \mid x := e; t \mid r \leftarrow x; t$ **threads**

$\mid \text{output } e \mid r \leftarrow \text{input}$

$\mid \text{if } (0 == e) \{t\} \{t\}$

$p ::= t \parallel \dots \parallel t$ **programs**

- ▶ Features *global variables* and *thread registers*
- ▶ Input / Output instructions used as “observation points”

Traditional LTS on states $\langle p \odot \mu : V \rightarrow \mathbb{N} \rangle$ labeled over:

$$\Sigma_{\text{SC}} ::= R_{x=k} \mid W_{x:=k} \mid O_k \mid I_k$$

Event structures

Definition

A Σ -**event structure** is a tuple $(E, \leq_E, \#_E, \text{lbl}_E : E \rightarrow \Sigma)$:

▶ (E, \leq_E) : a partial order representing *causality*

▶ $\#_E \subseteq E^2$: binary irreflexive relation representing *conflict*

+ axioms of *finite causes* and *conflict inheritance*.

$\rightsquigarrow \rightarrow$ is derived from \leq and \sim from $\#$.

A **configuration** of E is a subset $x \subseteq E$ which is:

▶ *downclosed* and *conflict-free*

$\mathcal{C}(E)$, the set of configurations of E is a LTS:

$$x \xrightarrow{a} y \quad \text{iff} \quad y = x \uplus \{e\} \wedge \text{lbl}(e) = a.$$

Overview of the semantics

Goal: produce $\llbracket \langle p \odot \mu \rangle \rrbracket_{sc}$ for each state such that:

$$\mathcal{C}(\llbracket \langle p \odot \mu \rangle \rrbracket_{sc}) \approx \langle p \odot \mu \rangle \quad \text{as } \Sigma_{sc}\text{-LTSs.}$$

4 steps:

- (1) Semantics of individual threads
- (2) Semantics of programs (without memory)
- (3) Semantics of memory
- (4) Combining the semantics.

Semantics of individual threads and memory

Individual threads. Using sums and prefixes:

$$\llbracket x := k; t \rrbracket_{sc} = W_{x:=k} \cdot \llbracket t \rrbracket_{sc}$$
$$\llbracket r \leftarrow x; t \rrbracket_{sc} = \sum_{n \in \mathbb{N}} R_{x=n} \cdot \llbracket t(n) \rrbracket_{sc}$$

The diagram illustrates the semantic derivation of the assignment and read operations. For the assignment operation, a prefix $W_{x:=k}$ is shown above a downward arrow pointing to the semantic expression $\llbracket t \rrbracket_{sc}$. For the read operation, a sum over $n \in \mathbb{N}$ is shown with a wavy line above it. Below the wavy line, two terms $R_{x=0}$ and $R_{x=1}$ are shown, each with a downward arrow pointing to its respective semantic expression $\llbracket t(0) \rrbracket_{sc}$ and $\llbracket t(1) \rrbracket_{sc}$.

Programs. Threads are combined using parallel composition

$$\llbracket t_1 \parallel \dots \parallel t_n \rrbracket_{sc} = \llbracket t_1 \rrbracket_{sc} \parallel \dots \parallel \llbracket t_n \rrbracket_{sc} \quad \llbracket t_1 \rrbracket_{sc} \dots \llbracket t_n \rrbracket_{sc}$$

Semantics of the memory

Storage semantics in SC orders accesses *on the same variable*.

$$m_{x:=k} = \begin{array}{cccc} R_{x:=k} & \overset{\text{~~~~~}}{\text{~~~~~}} & W_{x:=0} & \overset{\text{~~~~~}}{\text{~~~~~}} & W_{x:=1} & \dots \\ \downarrow & & \downarrow & & \downarrow & \\ m_{x:=k} & & m_{x:=0} & & m_{x:=1} & \dots \end{array}$$
$$[[\mu]] = m_{x:=\mu(x)} \parallel m_{y:=\mu(y)} \parallel \dots$$

$[[\mu]]$ is Σ_m -labelled ($\Sigma_m ::= R_{x:=k} \mid W_{x:=k}$).

More concretely:

- ▶ **Events** of $[[\mu]]$: consistent history *on one variable*.
- ▶ **Configurations** of $[[\mu]]$: consistent *global* history.

$[[\mu]]$ works for all multicopy atomics architectures.

Combining them: interaction states

$\llbracket \langle p \odot \mu \rangle \rrbracket$ should combine the behaviours of $\llbracket p \rrbracket$ and $\llbracket \mu \rrbracket$:

$$\begin{array}{ccc} W_{data:=17} & \xrightarrow{\llbracket \mu \rrbracket} & R_{flag=1} \\ \llbracket p \rrbracket \downarrow & & \downarrow \llbracket p \rrbracket \\ W_{flag:=1} & & R_{data=17} \end{array} \in \mathcal{C}(\llbracket \langle p \odot \mu \rangle \rrbracket)$$

Definition

A **synchronisation** is a tuple $X = (X.\text{thr}, X.\text{hist}, \varphi)$ with:

- ▶ $X.\text{thr} \in \mathcal{C}(\llbracket p \rrbracket)$ and $X.\text{hist} \in \mathcal{C}(\llbracket \mu \rrbracket)$.
- ▶ φ is a label-preserving bijection $X.\text{thr} \cap \Sigma_m \simeq X.\text{hist}$.

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There are two partial orders on $X.\text{thr}$:

$$s \leq_{\text{thr}(X)} s' := s \leq_{\llbracket p \rrbracket} s' \quad s \leq_{\text{mem}(X)} s' := \varphi s \leq_{\llbracket \mu \rrbracket} \varphi s'$$

X is **acyclic** when $\leq_{\text{thr}(X)} \cup \leq_{\text{mem}(X)}$ is acyclic.

The prime construction

Acyclic synchro. should be the configurations of $\llbracket \langle p \odot \mu \rangle \rrbracket$.

\rightsquigarrow In any E , $|E| \simeq \{x \in \mathcal{C}(E) \mid x \text{ has a greatest element}\}$.

Theorem (Prime construction, [Hay14])

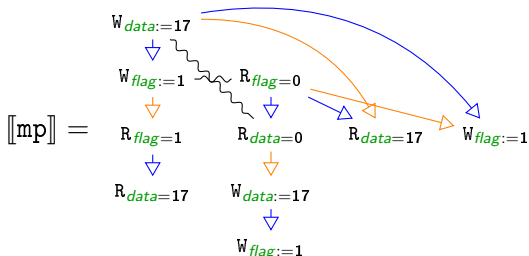
For a collection of partial orders \mathcal{Q} (closed under prefix), there exists an event structure $Pr(\mathcal{Q})$ such that $\mathcal{C}(Pr(\mathcal{Q})) \cong \mathcal{Q}$.

\rightsquigarrow Its events are elements of \mathcal{Q} with a greatest element.

We let $\llbracket p \rrbracket * \llbracket \mu \rrbracket$ to be the primes of acyclic configurations.

Correctness

$\llbracket p \rrbracket * \llbracket \mu \rrbracket$ can be equipped with two orders \leq_{thr} and \leq_{mem} .



Letting $\llbracket \langle p \odot \mu \rangle \rrbracket = \llbracket p \rrbracket * \llbracket \mu \rrbracket$ we have: $\llbracket \langle p \odot \mu \rangle \rrbracket \approx \langle p \odot \mu \rangle$.
 \rightsquigarrow Proof of correctness component by component.

II. A STRONG DRF RESULT FOR TSO

if p race-free on SC:

$$p \models_{SC} \varphi \Leftrightarrow p \models_{TSO} \varphi$$

Total Store Ordering in one slide [oss09]

TSO is a memory specification allowing for **store buffers**.

$$\begin{array}{c} x = y = 0. \\ x := 1 \parallel y := 1 \\ r \leftarrow y \parallel s \leftarrow x \\ \text{Allowed } r = s = 0. \end{array}$$

Usual LTS for TSO equips threads with a buffer in $(V \times \mathbb{N})^*$.

- ▶ New instruction, `fence`: flushes the current thread's buffer.
- ▶ New labels: $\Sigma_{\text{TSO}} := \Sigma_{\text{SC}} \mid \text{fence} \mid \text{BR}_{x:=k} \mid \text{BW}_{x:=k}$.

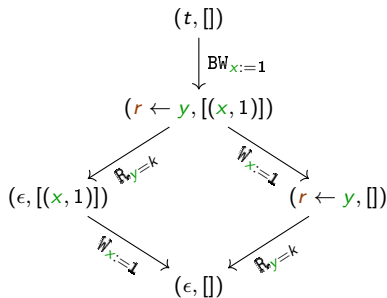
Our variations:

- ▶ Atomic accesses require empty buffers (as fences do)
- ▶ Input/Outputs do *not* require empty buffers.

Threads are not sequential anymore

For the thread $t = x := 1; r \leftarrow y$, a TSO processor may do:

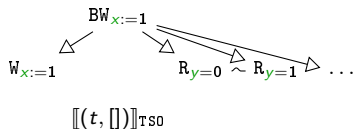
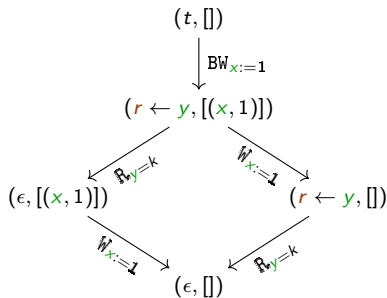
- ▶ Store the write, perform the read, commit the write.
- ▶ Commit directly the write and perform the read.



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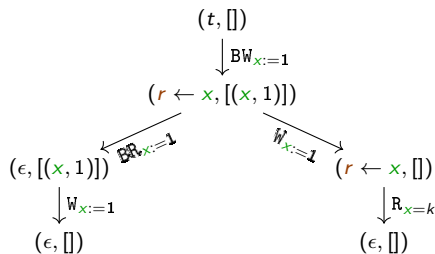
Events $W_{x:=1}$ and $R_{y=k}$ should be **concurrent** in $[(t, [])]_{TSO}$.

Threads are not deterministic anymore

For the thread $t = x := 1; r \leftarrow x$, a TSO processor may do:

- ▶ commit the write, and satisfy the read from memory
- ▶ store the write, read from the buffer and only then commit.

Those transitions are **not concurrent**.



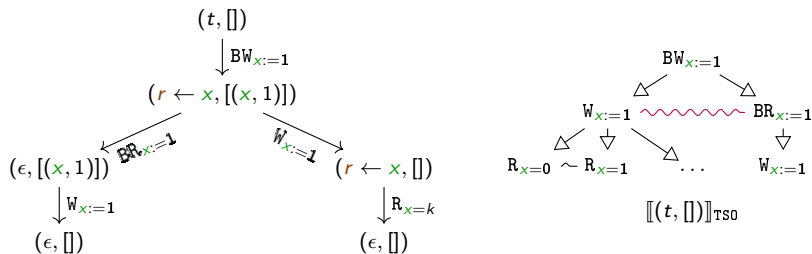
Events $W_{x:=1}$ and $BR_{x:=1}$ should be **in conflict** in $\llbracket (t, []) \rrbracket_{\text{TSO}}$.

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Generalised prefix and TSO thread semantics

To represent thread concurrency, we relax the usual prefix:

$$l \cdot_R E = \left(\begin{array}{c} \ell \\ \swarrow \quad \searrow \\ E \end{array} \right) : l \leq e \text{ when } (l, \text{lbl}(e')) \notin R \text{ for some } e' \leq e.$$

where $R \subseteq \Sigma \times \Sigma$ is the **concurrency relation**. For TSO:

$$R = \{(\text{W}_{x:=k}, e) \mid e \text{ I/O, read on nonatomic } y \neq x\}$$

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A few interesting rules:

$$\llbracket x := k; t, \mathbf{b} \rrbracket = \text{BW}_{x:=k} \cdot_R \llbracket t, \mathbf{b}++(x, k) \rrbracket$$

$$\llbracket \text{fence}; t, \mathbf{b} \rrbracket = \text{W}_{x_1:=k_1} \cdot_R \dots \cdot_R \text{W}_{x_n:=k_n} \cdot_R \text{fence} \cdot_R \llbracket t, \epsilon \rrbracket$$

$$\text{when } \mathbf{b} = [(x_1, k_1), \dots, (x_n, k_n)]$$

$$\llbracket r \leftarrow x; t, \mathbf{b} \rrbracket = (\text{BR}_{x:=k} \cdot_R \llbracket t[r := k], \mathbf{b} \rrbracket) + (\text{W}_{y:=m} \cdot_R \llbracket r \leftarrow x; t, \mathbf{b}' \rrbracket)$$

$$\text{when } x \text{ occurs in } \mathbf{b} \text{ with value } k \text{ and } \mathbf{b} = (y, m)++\mathbf{b}'.$$

Results about the TSO semantics.

The semantics extends to machines the same way as for SC:

$$\llbracket \langle \mathfrak{t}_1 \parallel \dots \parallel \mathfrak{t}_n \odot \mu \rangle \rrbracket_{\text{TSO}} = (\llbracket \mathfrak{t}_1 \rrbracket_{\text{TSO}} \parallel \dots \parallel \llbracket \mathfrak{t}_n \rrbracket_{\text{TSO}}) * \llbracket \mu \rrbracket$$

where \mathfrak{t}_i of the form (t_i, \mathfrak{b}_i)

Theorem

For any TSO machine state \mathfrak{m} , we have

$$\llbracket \mathfrak{m} \rrbracket_{\text{TSO}} \approx \mathfrak{m}.$$

Let us talk about races

Races are concurrent accesses on **nonatomic** variables.

Definition

A program p is **race-free** when for all $\langle p \odot \mu \rangle$ reducing to $\langle p' \odot \mu' \rangle$ (on SC), then p' does not have two initial actions on the same nonatomic variable one of which being a write.

This only allows thread communication on atomic variables:

Lemma

Let p be race-free and $e, e' \in \llbracket \langle p \odot \mu \rangle \rrbracket_{SC}$ such that:

- ▶ e and e' are not in conflict and not comparable for \leq_{thr} ,
- ▶ $e <_{\text{mem}} e'$ with no events in between.

Then e and e' are actions on an atomic variable.

Data-Race-Free theorem

We can generalise the result of [Owe10]:

Theorem

Let p be a race-free program. For any μ :

$$\mathcal{C}(\llbracket \langle p \odot \mu \rangle \rrbracket_{TSO}) \approx_{io} \mathcal{C}(\llbracket \langle p \odot \mu \rangle \rrbracket_{SC}),$$

\approx_{io} : weak bisimulation where visible events are IO events.

\rightsquigarrow satisfaction of Hennessy-Milner formulas is transferred.

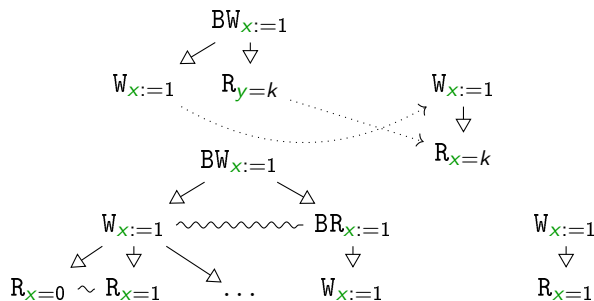
Among HML formulas, there are liveness properties, eg.

Program p inputs a natural number, outputs its double and then stops.

(NB: Trace based equivalences would allow p to stop after the input due to a deadlock.)

Outline of the proof

We first build a partial function $\psi : \llbracket p \rrbracket_{\text{Tso}} \rightarrow \llbracket p \rrbracket_{\text{sc}}$:



This function induces $\bar{\psi} : \mathcal{C}(\llbracket p \rrbracket_{\text{Tso}}) \rightarrow \mathcal{C}(\llbracket p \rrbracket_{\text{sc}})$.

Lemma

If p is race-free, $\bar{\psi}$ lifts to $\mathcal{C}(\llbracket \langle p \odot \mu \rangle \rrbracket_{\text{Tso}}) \rightarrow \mathcal{C}(\llbracket \langle p \odot \mu \rangle \rrbracket_{\text{sc}})$.

\rightsquigarrow The bisimulation is built using this map.

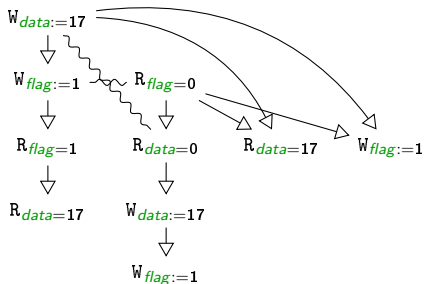
III. RELAXING COHERENCE

$$\begin{array}{ccc} W_{x:=1} & \sim & W_{x:=2} \\ \Downarrow & & \Downarrow \\ W_{x:=2} & & W_{x:=1} \end{array} \quad \text{vs.} \quad W_{x:=1} \quad W_{x:=2}$$

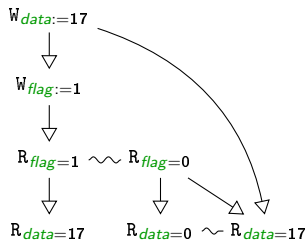
Coherence is too strict

Our memory cell $[[\mu]]$ orders every access to the same variable.

↪ Introduces undesired redundancy, eg. in mp:



Semantics of (1)



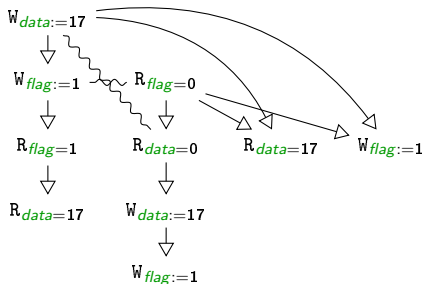
Optimised version

↪ Same outcomes but fewer configurations on the right.

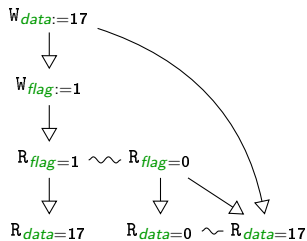
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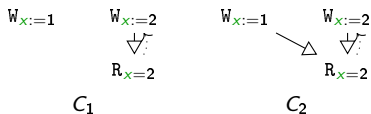
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Goal: Given E , build E_μ , a more compact version of $E * \llbracket \mu \rrbracket$?

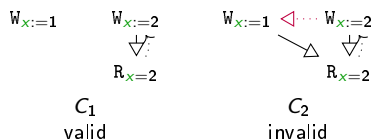
Our take on candidates

A **candidate** is a Σ -partial order where reads are justified:



Our take on candidates

A **candidate** is a Σ -partial order where reads are justified:



C is **valid** when all linearisations of writes are SC-executable.

Definition

An execution of $x \in \mathcal{C}(E)$ is a valid candidate C such that:

- (1) $|x| = |C|$ and $s \leq_E s' \Rightarrow s \leq_C s'$ for $s, s' \in x$
- (2) In C , I/O actions are all comparable.
- (3) It is minimal: there are no C' satisfying (1) and (2) with $\leq_C \subsetneq \leq_{C'}$.

The event structure E_μ

We can construct an event structure based on executions:

Theorem

*There exists an event structure E_μ whose **maximal** configurations correspond to pairs (x, C) of a maximal configuration of E and C an execution of x .*

Non-incremental: need the maximal configurations of E .

Theorem

- ▶ $tr_{io}(E_\mu) = tr_{io}(E * \llbracket \mu \rrbracket)$
- ▶ E_μ simulates $E * \llbracket \mu \rrbracket$.

$E * \llbracket \mu \rrbracket$ does not simulate E_μ : choices are made later in E_μ .

Approximating the executions

How to compute the executions of $x \in \mathcal{C}(E)$?

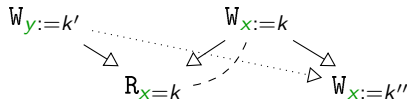
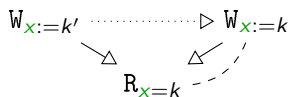
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1. Compute the possible justifications for reads in x . \rightsquigarrow A set of candidates C
2. For each C , add causal links to compute the possible executions augmenting C .

A simple heuristic, add links in the following cases:



(Heuristic independently developed by Luc Maranget)

This heuristic can be implemented in **Herd**.

\rightsquigarrow Ok for simple cases, but not for complicated programs...

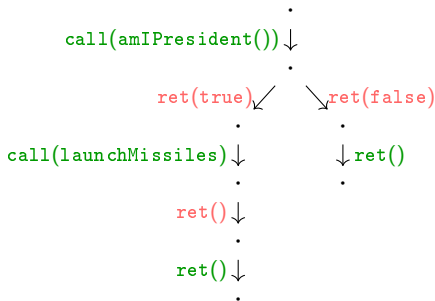
IV. BEYOND ASSEMBLY: HIGHER-ORDER LANGUAGES

Functions and LTS

What about code calling foreign functions?

```
void redButton (void) {  
    if (amIPresident())  
        launchMissiles();  
}
```

This can be described by a LTS using call/return events:

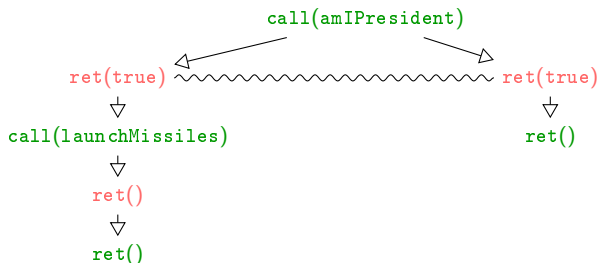


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}
```

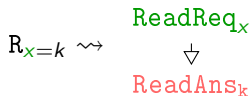
This can be described by a LTS using call/return events:



...or as an event structure.

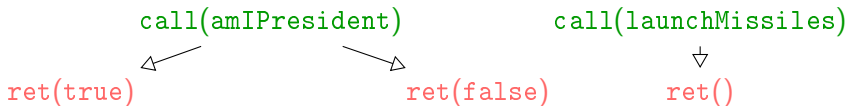
Labels organise themselves as games

- ▶ Labels are now **polarised** *Context/Program*:



- ▶ Labels have **rules**: “Do not return before you are called.”

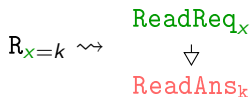
\rightsquigarrow Labels organise themselves in **games**: polarised forests.



A rule-preserving trace of a game is called a **play**.

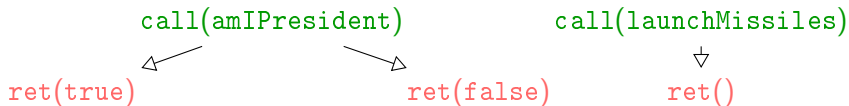
Labels organise themselves as games

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↪ Labels organise themselves in **games**: polarised forests.

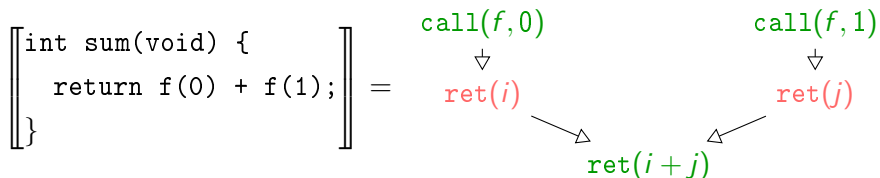


A rule-preserving trace of a game is called a **play**.

↪ **Game semantics** pioneered the study of programs as sets of plays on games (strategies) [HO00, AJM00].

Parallel functions as event structures

[RW11] used event structures to represent strategies:



↪ Opens the possibility to model open higher-order concurrent programs with event structures.

However, major restriction, **linearity**: in each configuration, each move must be played once!

Nonlinearity

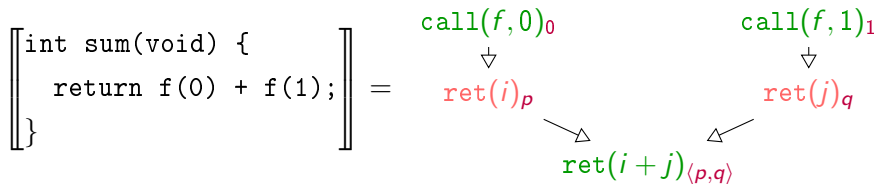
What if Player wants to be nonlinear?

↪ To call a function twice (as in the previous slide)

Following [AJM00], we add copy indices to moves:

game $A \rightsquigarrow$ game $!A$ where moves are duplicated ω times.

The previous example becomes:



A model of IPA

These considerations lead to:

Theorem (C., Clairambault, Winskel)

These expanded games and strategies form a model of higher-order concurrent and nondeterministic computation.

Model highlights the complicated causal patterns of such programs:

```
int shy(void){
  static int timesCalled = 0;
  timesCalled ++;
  if (timesCalled == 2) return 0;
  else while(true);
}
```

= 90 ...

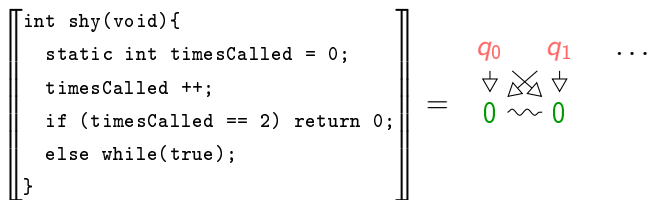
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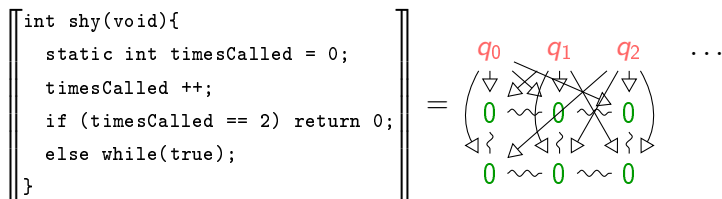
A model of IPA

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Related work

Weak memory and event structures.

- ▶ Brookes & Kavanagh's model of TSO with pomsets.
- ▶ Pichon & Sewell's operational semantics on event structures
- ▶ Jeffrey & Riely's axiomatic model using event structures

Game Semantics for concurrency.

- ▶ Laird, and Ghica & Murawski's models using interleaving.
- ▶ Tsukada & Sakayori's model of concurrency using set of pomsets.
- ▶ Hirschowitz's model using presheaves over spans.

A rich semantic universe based on event structures

Extensions. Model is extensible and has been extended to:

- ▶ continuous probabilities (Paquet, Winskel)
- ▶ quantum computation (Clairambault, de Visme, Winskel)

Ongoing work. In many different contexts:

- ▶ **probabilistic programming**
- ▶ **dependences of logical rules**
- ▶ **message-passing concurrency**

Research agenda.

- ▶ Investigate more applied models (ARM, C11), ...
- ▶ How to have a finite representation of these two issues:
 - ▶ recursion (depth)
 - ▶ unbounded contexts (breadth)
- ▶ Implement such models in a flexible way (à la Herd), ...

 Samson Abramsky, Radha Jagadeesan, and Pasquale Malacaria.

Full abstraction for PCF.

Information and Computation, 163(2):409–470, 2000.

 Jonathan Hayman.

Interaction and causality in digital signature exchange protocols.

In Matteo Maffei and Emilio Tuosto, editors, *Trustworthy Global Computing - 9th International Symposium, TGC 2014, Rome, Italy, September 5-6, 2014. Revised Selected Papers*, volume 8902 of *Lecture Notes in Computer Science*, pages 128–143. Springer, 2014.

 Martin Hyland and Luke Ong.

On full abstraction for PCF.

Information and Computation, 163:285–408, 2000.

 Scott Owens, Susmit Sarkar, and Peter Sewell.

A better x86 memory model: x86-tso.

In Theorem Proving in Higher Order Logics, 22nd International Conference, TPHOLs 2009, Munich, Germany, August 17-20, 2009. Proceedings, pages 391–407, 2009.



Scott Owens.

Reasoning about the implementation of concurrency abstractions on x86-tso.

In ECOOP 2010 - Object-Oriented Programming, 24th European Conference, Maribor, Slovenia, June 21-25, 2010. Proceedings, pages 478–503, 2010.



Silvain Rideau and Glynn Winskel.

Concurrent strategies.

In Proceedings of the 26th Annual IEEE Symposium on Logic in Computer Science, LICS 2011, June 21-24, 2011, Toronto, Ontario, Canada, pages 409–418, 2011.