Not so practical multicore programming

A simple model for sequential consistency, extended...

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Part 1.
Axiomatic Sequential Consistency

Shared memory computer

Thread$_1$  • • •  Thread$_n$

W  R

W  R

Shared Memory

Sequential consistency

Original definition: (Leslie Lamport)

[...] The result of any execution is the same as if the operations of all the processors were executed in some sequential order, and the operations of each individual processor appear in this sequence in the order specified by its program.

(And stores take effect immediately).

Interleaving semantics: This is “interleaving semantics” as “some sequential order” results from interleaving “the order specified by the program of all individual processors”.

At first, one expect shared multiprocessors to behave that way, which of course they don’t.
Formalism: events

The effect of “operations executed by the processors” are represented by events.

Operations we consider are the memory accesses. Hence, we define memory events \((a) d[\ell] v\), where:
- Unique label typically \((a), (b), \text{etc.}\)
- Direction \(d\), that is read (R) or write (W)
- Memory location \(\ell\), typically \(x, y, \text{etc.}\)
- Value \(v\), typically 0, 1 etc.
- Originating thread: \(T_0, T_1\) (usually omitted)

Formalism: program order

The program order \(\rightarrow\) is a total strict order amongst the events originating from the same processor.
Relation \(\rightarrow\) represents the sequential execution of events by one processor that follows the usual processor execution model, where instructions are executed by following the order given in program.

Example

```c
/* x, t and y are (shared) memory locations, t = \{ 2, 3, \} */
int r1, r2 = 0; // non-shared locations (e.g. registers)
x = 1;
for (int k = 0; k < 2; k++) { r1 = t[k]; r2 += r1; }
y = r2;
```

Events and program order:

\((a): W[x] 1 \rightarrow (b): R[t + 0] 2 \rightarrow (c): R[t + 4] 3 \rightarrow (d): W[y] 5\)

A definition of SC

A transcription of L. Lamport’s definition.

**Definition (SC 1)**

An execution is SC when there exists a total strict order on events \(<\), such that:
- Order \(<\) is compatible with program order:
  \[ e_1 \rightarrow \rightarrow e_2 \Rightarrow e_1 < e_2. \]
- Reads read from the closest write upwards (a.k.a. “most recent”):
  \[ \forall_{<} \text{ Def } \{ (w, r) | w = \max(w', \text{loc}(w')) = \text{loc}(r) \land w' < r \}. \]

Example of a question on SC

<table>
<thead>
<tr>
<th>(R)</th>
<th>(T_0)</th>
<th>(T_1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>((a) x \leftarrow 1)</td>
<td>((b) y \leftarrow 1)</td>
<td>((c) y \leftarrow 2)</td>
</tr>
<tr>
<td>((d) x_0 \leftarrow x)</td>
<td>(\text{Observed? } y=2, x_0=0)</td>
<td></td>
</tr>
</tbody>
</table>

How do we know? Let us enumerate all interlavings:

\[ a, b, c, d \quad y=2, x_0=1; \]
\[ a, c, b, d \quad y=1, x_0=1; \]
\[ a, c, d, b \quad y=1, x_0=1; \]
\[ c, d, a, b \quad y=1, x_0=0; \]
\[ c, a, b, d \quad y=1, x_0=1; \]
\[ c, a, d, b \quad y=1, x_0=1; \]

Remark: if \(b < c\) then \(y=2\), if \(a < d\) then \(x_0=1\).
Let us be a bit more clever

<table>
<thead>
<tr>
<th></th>
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<th>( T_1 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( a )</td>
<td>( x \leftarrow 1 )</td>
<td>( c )</td>
</tr>
<tr>
<td>( b )</td>
<td>( y \leftarrow 1 )</td>
<td>( d )</td>
</tr>
</tbody>
</table>

Observed? \( y = 2 \); \( r_0 = 0 \)

Collecting constraints on the scheduling order \(<\):

We respect program order, thus \( a < b \), \( c < d \).
We observe \( r_0 = 0 \), thus \( d < a \), as \( d \) reads initial value, which is overwritten by \( a \).
We observe \( y = 2 \), thus \( b < c \).

Hence we have a cycle in \(<\), which prevents it from being an order!

\[ a < b < c < d < a \cdots \]

**Conclusion:** No SC execution would ever yield the output "\( y = 2 \); \( r_0 = 0 \)."

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**Systematic approach**

At the moment, an "execution" (candidate) consists in assuming some events and a program order relation.

We assume two additional relations:

- **Read-from** \( \leftarrow \rf \): Relates write events to read events that read the stored value (initial writes left implicit in diagrams).
  \[ \forall r, \exists! w, w \rightarrow r \]
  *(Notice: \( w \) and \( r \) have identical location and value.)*

- **Coherence** \( \rightarrow \co \): Relates write events to the same location.
  For any location \( \ell \), the restriction of \( \rightarrow \co \) to write events to location \( \ell \) \((W_\ell)\) is a total strict order.

---

**Coherence as a characteristics of shared memory**

The very existence of \( \rightarrow \co \) is implied by the existence of a shared, coherent, memory — Given location \( x \), there is exactly one memory cell whose location is \( x \).

\[ Wx_0 \rightarrow \co Wx_1 \rightarrow x = 2 \rightarrow \co Wx_3 \rightarrow \cdots \]

Of course, in reality, there caches, buffers etc. But the system will behave "as if".

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**Example of \( \rightarrow \rf \)**

<table>
<thead>
<tr>
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<th>( T_0 )</th>
<th>( T_1 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( a )</td>
<td>( r_0 \leftarrow x )</td>
<td>( c )</td>
</tr>
<tr>
<td>( b )</td>
<td>( y \leftarrow 1 )</td>
<td>( d )</td>
</tr>
</tbody>
</table>

Observed: \( r_0 = 0; r_1 = 1; \)

There are 4 possible \( \rightarrow \rf \) relations (initial value is 0).

\[ r_0 = 1; r_1 = 1; \quad r_0 = 1; r_1 = 0; \]

- \( a \): \( Rx = 1 \) \( \rightarrow \rf \) \( Rp \)
- \( b \): \( Wy = 1 \) \( \rightarrow \rf \) \( Rp \)
- \( c \): \( Ry = 1 \) \( \rightarrow \rf \) \( Rp \)
- \( d \): \( Wx = 1 \) \( \rightarrow \rf \) \( Rp \)

\[ r_0 = 0; r_1 = 1; \quad r_0 = 0; r_1 = 0; \]

- \( a \): \( Rx = 0 \) \( \rightarrow \rf \) \( Rp \)
- \( b \): \( Wy = 1 \) \( \rightarrow \rf \) \( Rp \)
- \( c \): \( Ry = 0 \) \( \rightarrow \rf \) \( Rp \)
- \( d \): \( Wx = 1 \) \( \rightarrow \rf \) \( Rp \)
Example of $\xrightarrow{\text{co}}$

$$
\begin{array}{c|c|c|c|c}
2+2W \\
\hline
T_0 & T_1 \\
\hline
(a) x \leftarrow 2 & (c) y \leftarrow 2 \\
(b) y \leftarrow 1 & (d) x \leftarrow 1 \\
\hline
\text{Observed? } x=2; y=2; \\
\end{array}
$$

x=1; y=2;  
\begin{align*}
(a) & \text{ } & c: Wx=2 & \text{ \text{co}} \rightarrow (\text{co}) \\
\text{por} & \text{ } & b: Wy=1 & \text{ \text{co}} \rightarrow (\text{co}) \\
\text{por} & \text{ } & d: Wx=1 & \text{ \text{co}} \rightarrow (\text{co}) \\
\end{align*}

$\text{Observed? } x=2; y=2; \\
\begin{align*}
(a) & \text{ } & c: Wx=2 & \text{ \text{co}} \rightarrow (\text{co}) \\
\text{por} & \text{ } & b: Wy=1 & \text{ \text{co}} \rightarrow (\text{co}) \\
\text{por} & \text{ } & d: Wx=1 & \text{ \text{co}} \rightarrow (\text{co}) \\
\end{align*}

$\text{Notice: }$ In this simple case of two stores, the value finally observed in locations determines $\xrightarrow{\text{co}}$ for them.

One more relation: $\xrightarrow{\text{fr}}$

The new relation $\xrightarrow{\text{fr}}$ (from read) relates reads to “younger writes” (younger w.r.t. $\xrightarrow{\text{co}}$).

$$
\begin{align*}
& r \xrightarrow{\text{fr}} w & \overset{\text{Def}}{=} w' \xrightarrow{\text{fr}} r \land w' \xrightarrow{\text{co}} w \\
\end{align*}
$$

This amounts to place a read into the coherence order of its location:

$$
\begin{align*}
& r \xrightarrow{\text{fr}} w & \overset{\text{Def}}{=} w' \xrightarrow{\text{fr}} r \land w' \xrightarrow{\text{co}} w \\
\end{align*}
$$

We have

$$
\begin{align*}
& w_0 \xrightarrow{\co} w_1 \xrightarrow{\co} \ldots \xrightarrow{\co} w_n \\
\end{align*}
$$

(Or: $\xrightarrow{\text{fr}} \overset{\text{Def}}{=} (\xrightarrow{\text{fr}})^{-1} \land \xrightarrow{\text{co}}$)

Second definition of SC

Definition (SC 2)

An execution is SC when:

$$
\text{Acyclic } \left( \xrightarrow{\text{fr}} \cup \xrightarrow{\text{co}} \cup \xrightarrow{\text{fr}} \cup \xrightarrow{\text{po}} \right)
$$

And of course:

The two definitions of SC are equivalent.
SC 1 $\implies$ SC 2

Assume the existence of the total order “$<$”.
Define: \[ \text{co} \overset{\text{Def}}{=} \{(w_1, w_2) | \text{loc}(w_1) = \text{loc}(w_2) \land w_1 < w_1\} \]

Notice that $\text{rf} \overset{\text{Def}}{=} \text{co}$ is already defined: $\text{co} \subseteq <$. Also notice $\text{po} \subseteq <$, $\text{co} \subseteq <$ and $\text{rf} \subseteq <$.

Proof:
Define $\text{fr} \overset{\text{Def}}{=} \text{rf}^{-1}$; $\text{co}$, and prove $\text{fr} \subseteq <$. Let $r \overset{\text{fr}}{=} w$. Let further $w_0 \overset{\text{co}}{=} r$, then, by definition of $\text{fr}$, we have $w_0 \overset{\text{co}}{=} w$ and thus $w_0 < w$.

But, $w_0$ is maximal amongst all $w' < r$. That is: “$w < r \implies w \leq w_0$” or, “$w_0 < w \implies r < w$” QED.

Hence, a cycle in $\text{rf} \cup \text{co} \cup \text{fr} \cup \text{po}$ would be a cycle in order “$<$”

Simulating SC

Which model, SC 1 or SC 2 is the most convenient/efficient?

SC 1 Enumerate interleavings.

SC 2 Enumerate axiomatic execution candidates (i.e. $\text{po} \setminus \text{rf} \setminus \text{co}$); check the acyclicity of $\text{rf} \cup \text{co} \cup \text{fr} \cup \text{po}$.

Answer: we view SC 2 as being more convenient, since the generated objects usually are smaller.

Introducing herd, a memory model simulator

A model sc.cat:

```% cat sc.cat
include "cos.cat" #define co (and fr as "rf^{-1}; co")
let com = rf | co | fr #communication
acyclic po | com as hb #validity condition
```

Running R on SC (demo in demo/herd):

```% herd7 -cat sc.cat R.litmus
Test R Allowed States 3
1:EAX=0; y=1;
1:EAX=1; y=1;
1:EAX=1; y=2;
```

No Witnesses

Positive: 0 Negative: 3

Condition exists (y=2 / \ 1:EAX=0)

Observation R Never 0 3

Notice: Outcome 1:EAX=0; y=2; is forbidden by SC.
Herd structure

Generate all candidate executions, i.e. all possible $\text{po} \rightarrow$, $\text{rf} \rightarrow$ and $\text{co} \rightarrow$ (with $\fr$ deduced):

- a: $Wx=1$
- b: $Wy=1$
- c: $Wy=2$
- d: $Rx=0$

Ok

No

Apply model checks to each candidate execution.

Part 2.

Studying Non-Sequentially Consistent Executions.

Violations of SC

A cycle of $\text{po} \rightarrow$, $\text{rf} \rightarrow$, $\text{co} \rightarrow$, $\fr$ describes a violation of SC. From such a cycle, one may easily generate programs that potentially violate SC, and run them on actual machines.

However, the cycle does not describe:
- How many threads are involved.
- How many memory locations are involved.

We now aim at:
- Extract a subset of significant cycles.
- Generate one program out of one cycle.

Simplifying cycles: $\text{po} \rightarrow$ and $\text{com} \rightarrow$ steps alternate

A cycle in $\text{com} \rightarrow \cup \text{po} \rightarrow$ is a cycle in $\text{po} \rightarrow^+ \cup \text{com}^+$ (group $\text{po} \rightarrow$ and $\text{com} \rightarrow$ steps together). Then:
- $\text{po} \rightarrow$ is transitive $\text{po} \rightarrow^+ \subseteq \text{po} \rightarrow$.
- $\text{com}^+$ is the union of the five following relations:

$$
\text{com}^+ = \text{rf} \rightarrow \cup \text{co} \rightarrow \cup \text{fr} \rightarrow \cup (\text{co} \rightarrow;\text{rf} \rightarrow) \cup (\text{fr} \rightarrow;\text{rf} \rightarrow).
$$

Because $(\text{co} \rightarrow; \text{co} \rightarrow) \subseteq \text{co} \rightarrow$, $(\text{fr} \rightarrow; \text{co} \rightarrow) \subseteq \text{fr} \rightarrow$, and $(\text{rf} \rightarrow; \text{fr} \rightarrow) \subseteq \text{co} \rightarrow$.

**Conclusion:** Any cyclic $\text{com} \rightarrow \cup \text{po} \rightarrow$ includes a cycle in $\text{po} \rightarrow^+ \cup \text{com}^+$ — i.e. that alternates $\text{po} \rightarrow$ steps and $\text{com} \rightarrow$ steps.
Simplifying cycles: all \( \text{com} \) steps are external

Given a cycle, we consider that all \( \text{com} \) and \( \text{\hat{com}} \) steps are external, \( \text{i.e.} \) source and target events are from pairwise distinct threads.

Given \( e_1 \xrightarrow{\text{com}} e_2 \), s.t. \( e_1 \) and \( e_2 \) are from the same thread:
- Either \( e_1 \xrightarrow{\text{po}} e_2 \) and we consider this \( \text{po} \) step in the cycle, in place of the \( \text{com} \) step (further merging \( \text{po} \) steps to get a smaller cycle).
- Or \( e_2 \xrightarrow{\text{po}} e_1 \), then we have a very simple cycle \( e_2 \xrightarrow{\text{po}} e_1 \xrightarrow{\text{\hat{com}}} e_2 \).
Such cycles are “violations of coherence” (more on them later).

\[ \text{Case } e_1 = e_2 \text{ is impossible (\( \text{com} \) is acyclic, see later)} \]

Notice: A similar reasoning applies to individual \( \text{com} \) steps in composite \( \text{\hat{com}} \).

Test from cycles — Threads

Cycle: \( R \xrightarrow{\text{po}} W \xrightarrow{\text{rf}} R \xrightarrow{\text{po}} W \xrightarrow{\text{rf}} R \xrightarrow{\text{po}} W \xrightarrow{\text{rf}} R \xrightarrow{\text{po}} W \xrightarrow{\text{rf}} \)

Consider a test execution on two threads:
The test execution features a smaller cycle

- a: \( Rx=1 \) \( \xrightarrow{\text{po}} \) e: \( Ry=1 \) \( \xrightarrow{\text{po}} \)
- b: \( Wy=1 \) \( \xrightarrow{\text{po}} f: \( Wz=1 \) \( \xrightarrow{\text{po}} \)
- c: \( Rz=1 \) \( \xrightarrow{\text{po}} g: \( Ra=1 \) \( \xrightarrow{\text{po}} \)
- d: \( Wa=1 \) \( \xrightarrow{\text{po}} h: \( Wx=1 \) \( \xrightarrow{\text{po}} \)

Generally: one passage per thread

Test from cycles — Locations

Cycle: \( R \xrightarrow{\text{po}} W \xrightarrow{\text{rf}} R \xrightarrow{\text{po}} W \xrightarrow{\text{rf}} R \xrightarrow{\text{po}} W \xrightarrow{\text{rf}} R \xrightarrow{\text{po}} W \xrightarrow{\text{rf}} \)

- One interpretation (four locations):
  - a: \( Rx=1 \) \( \xrightarrow{\text{po}} \) 
  - c: \( Ry=1 \) \( \xrightarrow{\text{po}} \)
  - e: \( Rz=1 \) \( \xrightarrow{\text{po}} \)
  - g: \( Ra=1 \) \( \xrightarrow{\text{po}} \)

- Another interpretation (two locations):
  - a: \( Rx=2 \) \( \xrightarrow{\text{po}} \)
  - c: \( Ry=1 \) \( \xrightarrow{\text{po}} \)

Assuming a cycle with two \( \text{po} \) steps on the same thread:

\[ e_1 \xrightarrow{\text{po}} e_2 \xrightarrow{\text{com}} e_3 \xrightarrow{\text{po}} e_4 \xrightarrow{\text{com}} e_5 \xrightarrow{\text{po}} e_1 \]

Assuming for instance, \( e_1 \xrightarrow{\text{po}} e_3 \) then we have a “simpler” cycle:

\[ e_1 \xrightarrow{\text{po}} e_3 \xrightarrow{\text{po}} e_4 \xrightarrow{\text{com}} \xrightarrow{\text{po}} e_5 \xrightarrow{\text{po}} e_1 \]

(Conclude with \( \text{po} \) being transitive)

If \( e_1 = e_3 \), we also have a simpler cycle:

\[ e_1 \xrightarrow{\text{po}} e_1 \]

Conclusion: Cycle visit a thread at most once.
The second interpretation is not “minimal”

Assume a cycle including locations are related by complex steps. By the identical locations lemma:

- Either, \( e_1 \xrightarrow{\text{com}} e_2 \) or \( e_2 \xrightarrow{\text{com}} e_1 \), and we have a smaller cycle.
- Or, \( w \xrightarrow{\text{rf}} e_1 \) and \( w \xrightarrow{\text{rf}} e_2 \), see next page!

Generally: do not repeat locations in cycles.

Simplifying cycles – Identical Locations

We show that we can restrict cycles to those where events with identical locations are related by \( \xrightarrow{\text{com}} \) steps.

Assume a cycle including \( e_1 \) and \( e_2 \) with the same location.

- If \( e_1 \) and \( e_2 \) are from different threads. By hypothesis, \( e_1 \) and \( e_2 \) are related by complex steps (i.e. at least one \( \xrightarrow{\text{po}} \) and one \( \xrightarrow{\text{com}} \)) in both directions. By the identical locations lemma:
  - Either, \( e_1 \xrightarrow{\text{com}} e_2 \) or \( e_2 \xrightarrow{\text{com}} e_1 \), and we have a smaller cycle.
  - Or, \( w \xrightarrow{\text{rf}} e_1 \) and \( w \xrightarrow{\text{rf}} e_2 \). — see next page!

- If \( e_1 \) and \( e_2 \) are from the same thread, i.e. for instance \( e_1 \xrightarrow{\text{po}} e_2 \), while \( e_2 \) relates to \( e_1 \) by complex steps:
  - either \( e_1 \xrightarrow{\text{com}} e_2 \) and we replace the \( \xrightarrow{\text{po}} \) step in cycle, yielding a simpler cycle (one \( \xrightarrow{\text{po}} \), \( \xrightarrow{\text{com}} \) step less)
  - or \( e_2 \xrightarrow{\text{com}} e_1 \) and we have a very simple cycle \( e_1 \xrightarrow{\text{po}} e_2 \xrightarrow{\text{com}} e_1 \).
  - Or \( w \xrightarrow{\text{rf}} e_1 \) and \( w \xrightarrow{\text{rf}} e_2 \), we short-circuit the cycle — as the cycle must be \( \cdots w \xrightarrow{\text{rf}} e_1 \xrightarrow{\text{po}} e_2 \cdots \), which we reduce into \( \cdots w \xrightarrow{\text{rf}} e_2 \cdots \).

Simplifying cycles, a lemma

**Lemma (Identical locations)**

Let \( e_1, e_2 \) two different events with the same location,

- either \( e_1 \xrightarrow{\text{com}} e_2 \),
- or \( e_2 \xrightarrow{\text{com}} e_1 \),
- or \( w \xrightarrow{\text{rf}} e_1 \) and \( w \xrightarrow{\text{rf}} e_2 \).

Case analysis:

- \( w_1, w_2 \), then either \( w_1 \xrightarrow{\text{co}} w_2 \) or \( w_2 \xrightarrow{\text{co}} w_1 \) (total order).
- \( r_1, r_2 \), let \( w_1 \xrightarrow{\text{rf}} r_1 \) and \( w_2 \xrightarrow{\text{rf}} r_2 \). Then, either \( w_1 = w_2 \) and we are in case 3; or (for instance) \( w_1 \xrightarrow{\text{co}} w_2 \) and we have \( r_1 \xrightarrow{\text{fr}} w_2 \xrightarrow{\text{rf}} r_2 \).
- \( r_1, w_2 \), let \( w_1 \xrightarrow{\text{rf}} r_1 \). Then, either \( w_1 = w_2 \) and \( w_2 \xrightarrow{\text{rf}} r_1 \); or \( w_1 \xrightarrow{\text{co}} w_2 \) and \( r_1 \xrightarrow{\text{fr}} w_2 \); or \( w_2 \xrightarrow{\text{co}} w_1 \) and \( w_2 \xrightarrow{\text{co}} \xrightarrow{\text{rf}} r_1 \).

**Corollary:** \( \xrightarrow{\text{com}} \) is acyclic.

Next page

So let us assume a cycle that includes \( r_1 \) and \( r_2 \), related in both directions by complex steps and such that \( w \xrightarrow{\text{rf}} r_1 \) and \( w \xrightarrow{\text{rf}} r_2 \). We consider:

- If \( w \xrightarrow{\text{rf}} r_1 \) is in cycle, then there is an obvious short-circuit: replace \( \xrightarrow{\text{rf}} \) followed by the complex steps from \( r_1 \) to \( r_2 \) by a single \( w \xrightarrow{\text{rf}} r_2 \) step.
- If \( w \xrightarrow{\text{rf}} r_2 \) is in cycle, symmetrical case.
- Otherwise, it must be that both \( r_1 \) and \( r_2 \) are the target of \( \xrightarrow{\text{po}} \) steps and the source of \( \xrightarrow{\text{fr}} \) steps: let \( w_1 \) and \( w_2 \) be the targets of those steps.

Then, in all possible three situations: \( w = w_2, w_1 \xrightarrow{\text{co}} w_2 \) and \( w_2 \xrightarrow{\text{co}} w_1 \) we construct a simpler cycle that does not contain \( r_1 \) or \( r_2 \).
In a non SC execution we find:

- A violation of coherence, that is a cycle $e_1 \xrightarrow{po} e_2 \xrightarrow{com} e_1$.
- Or a critical cycle that is:
  - The cycle alternates $po$ steps and external $com$ steps.
  - The cycle passes through a given thread at most once.
  - All $com$ steps have pairwise different locations.
  - The source and target of one given $po$ steps have different locations.

Notice: By the last condition, such cycles have four steps or more and pass through two threads or more.

Application, all possible SC violations on two threads

Simply list all (critical) cycles for 2 threads, we have six cycles:

- **2+2W**: $po \xrightarrow{co} po \xrightarrow{co}$
- **LB**: $po \xrightarrow{rf} po \xrightarrow{rf}$
- **MP**: $po \xrightarrow{rf} po \xrightarrow{fr}$
- **R**: $po \xrightarrow{co} po \xrightarrow{co}$
- **S**: $po \xrightarrow{fr} po \xrightarrow{fr}$
- **SB**: $po \xrightarrow{fr} po \xrightarrow{fr}$

Any non-SC execution on two threads includes one of the above six cycles.

Notice: up to coherence violations (previous slide).
### Application

We assume the following on modern shared memory architectures:

- No valid execution includes a violation of coherence.
- No valid execution includes a cycle whose $\rightarrow$ steps include the adequate fence instruction between source and target instructions.
- The full memory barrier is always adequate.

To guarantee SC:

- Find all possible critical cycles of all possible executions on the architecture.
- Insert a fence in every $\rightarrow$ step of those.

Simplification:

- Insert fences between all pairs of racy accesses with different locations (notice that $\rightarrow$ always includes a write).

Optimisation:

- Forbid specific (critical) cycles by specific means (lightweight barriers, dependencies).

### A semi realistic example

```c
for (int k = N ; k >= 0 ; k--) {
    a: x = k ;
    sync() ;
    b: go = 1 ;
    c: while (go == 1) ;
    sync() ;
    d: while (go == 0) ;
    e: int t = x; sum += t;
    f: go = 0 ;
}
```

To insert fence, consider separating accesses to go and x.

```c
for (int k = N ; k >= 0 ; k--) {
    a: x = k ;
    sync() ;
    b: go = 1 ;
    c: while (go == 1) ;
    sync() ;
    d: while (go == 0) ;
    sync() ;
    e: int t = x; sum += t;
    sync() ;
    f: go = 0 ;
}
```
A semi realistic example, more precise fencing

```c
for (int k = N; k >= 0; k--) {
    a: x = k;
    b: go = 1;
    c: while (go == 1);
}

int sum = 0;
for (int k = N; k >= 0; k--) {
    a: while (go == 0);
    b: sum += x;
    c: go = 0;
}
```

The resulting static $\mathcal{G}_0$ relation is as follows.

<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>a</td>
<td>v</td>
<td>l</td>
<td>0</td>
<td>w</td>
<td>l</td>
</tr>
<tr>
<td>b</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>c</td>
<td>0</td>
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<tr>
<td>d</td>
<td>0</td>
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<tr>
<td>e</td>
<td></td>
<td></td>
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<td></td>
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</tbody>
</table>

Analysis based upon Sekar et al. Power model (PLDI’11). Test **MP**

\[
\begin{align*}
\text{X86: } & \quad \text{no fence needed.}
\end{align*}
\]

**Cycle 1**

\[
\begin{align*}
a: W[x] &= v \quad & d: R[go] &= 1 \\
b: W[go] &= 1 \quad & e: R[x] &= w \\
c: R[go] &= 0 \quad & f: W[go] &= 0 \\
\end{align*}
\]

Analysis based upon Sekar et al. Power model (PLDI’11). Test **MP**

\[
\begin{align*}
\text{X86: } & \quad \text{no fence needed.}
\end{align*}
\]

**Cycle 2**

\[
\begin{align*}
a: W[x] &= v \quad & d: R[go] &= 1 \\
b: W[go] &= 1 \quad & e: R[x] &= w \\
c: R[go] &= 0 \quad & f: W[go] &= 0 \\
\end{align*}
\]

Analysis based upon Sekar et al. Power model (PLDI’11). Test **R**

\[
\begin{align*}
\text{X86: } & \quad f \xrightarrow{\text{mfence}} e
\end{align*}
\]

**Cycle 3**

\[
\begin{align*}
a: W[x] &= v \quad & d: R[go] &= 1 \\
b: W[go] &= 1 \quad & e: R[x] &= w \\
c: R[go] &= 0 \quad & f: W[go] &= 0 \\
\end{align*}
\]

Analysis based upon Sekar et al. Power model (PLDI’11). Test **SB**

\[
\begin{align*}
\text{X86: } & \quad a \xrightarrow{\text{sync}} c, f \xrightarrow{\text{sync}} e
\end{align*}
\]
Cycle 4

\[
\begin{align*}
\text{a: } & W[x] = v \\
\text{b: } & W[go] = 1 \\
\text{c: } & R[go] = 0 \\
\text{d: } & R[go] = 1 \\
\text{e: } & R[x] = w \\
\text{f: } & W[go] = 0
\end{align*}
\]

Analysis based upon Sekar et al. Power model (PLDI’11). Test MP

\[
\begin{align*}
\text{b} & \xrightarrow{\text{lwsync}} \text{a}, \text{e} & \xrightarrow{\text{ctfsync}} \text{d}
\end{align*}
\]

X86: no fence needed.

Cycle 5

\[
\begin{align*}
\text{a: } & W[x] = v \\
\text{b: } & W[go] = 1 \\
\text{c: } & R[go] = 0 \\
\text{d: } & R[go] = 1 \\
\text{e: } & R[x] = w \\
\text{f: } & W[go] = 0
\end{align*}
\]

Analysis based upon Sekar et al. Power model (PLDI’11). Test S

\[
\begin{align*}
\text{b} & \xrightarrow{\text{lwsync}} \text{a}, \text{e} & \xrightarrow{\text{ctrl}} \text{f}
\end{align*}
\]

X86: no fence needed.

Cycle 6

\[
\begin{align*}
\text{a: } & W[x] = v \\
\text{b: } & W[go] = 1 \\
\text{c: } & R[go] = 0 \\
\text{d: } & R[go] = 1 \\
\text{e: } & R[x] = w \\
\text{f: } & W[go] = 0
\end{align*}
\]

Analysis based upon Sekar et al. Power model (PLDI’11). Test LB

\[
\begin{align*}
\text{c} & \xrightarrow{\text{ctrl}} \text{a}, \text{e} & \xrightarrow{\text{ctrl}} \text{f}
\end{align*}
\]

X86: no fence needed.

Sufficient fencing, X86

\[
\begin{align*}
\text{for } & \left(\text{int } k = N ; k >= 0 ; k--\right) \{ \\
\text{a: } & x = k \\
\text{b: } & \text{mfence}() \\
\text{c: } & \text{while } (go == 1) \\
\text{d: } & \text{while } (go == 0) \\
\text{e: } & \text{int } t = x; \text{sum} += t \\
\text{f: } & \text{go} = 0 \\
\text{g: } & \text{mfence}()
\end{align*}
\]

\[\text{Notice: Inserting full memory fence between racy writes gives the same result.}\]
for (int k = N ; k >= 0 ; k--) {
    a: x = k ;
    sync() ;
    b: go = 1 ;
    c: while (go == 1) ;
        lwsync() ;
    
    int sum = 0 ;
    for (int k = N ; k >= 0 ; k--) {
        d: while (go == 0) ;
            sync() ;
        e: int t = x; sum += t;
            ctrlisync(t) ;
        f: go = 0 ;
    }
}

Notice: Inserting full memory fence between racy accesses is much more simple.

**Part 3.**

**Axiomatic TSO**

**TSO — The Model of X86 machines**

The write buffer explains how "reads can pass over writes".
**Results for running the six test on this machine**

```
<table>
<thead>
<tr>
<th>Action</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>a: Wx=1</td>
<td>c: Wy=2</td>
</tr>
<tr>
<td>b: Wy=1</td>
<td>d: Rx=0</td>
</tr>
<tr>
<td>a: Wx=1</td>
<td>c: Wy=1</td>
</tr>
<tr>
<td>b: Wy=1</td>
<td>d: Rx=1</td>
</tr>
<tr>
<td>a: Wx=1</td>
<td>c: Wy=2</td>
</tr>
<tr>
<td>b: Wy=1</td>
<td>d: Rx=1</td>
</tr>
</tbody>
</table>

R: Ok  S: No  SB: Ok
```

**Restoring SC with mfence**

Replace “relaxed” (not in HBB) WR(po) by mfence (in HBB).

```
<table>
<thead>
<tr>
<th>T0</th>
<th>T1</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) x ← 1</td>
<td>(c) y ← 2</td>
</tr>
<tr>
<td>(b) y ← 1</td>
<td>(d) r0 ← x</td>
</tr>
</tbody>
</table>
```

Observed? y=2; r0=0

<table>
<thead>
<tr>
<th>T0</th>
<th>T1</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) x ← 1</td>
<td>(c) y ← 1</td>
</tr>
<tr>
<td>(b) r0 ← y</td>
<td>(d) r1 ← x</td>
</tr>
</tbody>
</table>
```

Observed? r0=0; r1=0

No

**Axiomatic TSO, model TSO 1**

- Remember SC:
  
  \[ \text{Acyclic } \left(\frac{r}{c} \cup \frac{c}{r} \cup \frac{r}{c} \cup \frac{c}{r} \cup \frac{c}{r} \cup \frac{c}{r} \right) \]

  A model for herd, our generic simulator:

  let ppo = po # ppo stands for 'preserved program-order'
  let com-hb = fr | rf | co # All communications create order
  acyclic (ppo | com-hb)

- In TSO:
  
  - Write-to-read does not create order:
    
    let ppo = (R*W | W*W) & po # All pairs except W*R pairs
  - Communication create order
    
    let com-hb = rf | co | fr

- TSO “happens-before” (HBB) check:
  
  \[ \text{acyclic } (ppo | \text{com-hb} | \text{mfence}) \text{ as } \text{hb} \]

**Notice:** Relations can be interpreted as being between the points in time where a load binds its value and where a written value reaches memory.
Our TSO 1 model is wrong!

Consider:

<table>
<thead>
<tr>
<th>SB+rfi-pos</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_0$</td>
<td>$T_1$</td>
</tr>
<tr>
<td>$(a) x \leftarrow 1$</td>
<td>$(d) y \leftarrow 1$</td>
</tr>
<tr>
<td>$(b) r0 \leftarrow x$</td>
<td>$(e) r2 \leftarrow y$</td>
</tr>
<tr>
<td>$(c) r1 \leftarrow y$</td>
<td>$(f) r3 \leftarrow x$</td>
</tr>
</tbody>
</table>

Observed? $r0=1; r1=0; r2=1; r3=0$;

According to model? No. As we have the hb cycle:

$$a \xrightarrow{rf} b \xrightarrow{po} c \xrightarrow{fr} d \xrightarrow{rf} e \xrightarrow{po} f \xrightarrow{fr} a$$

According to experiments? Ok. Hence TSO 1 is invalidated by hardware.

The effect originates from "store forwarding": A thread can read its own writes from its store buffer, i.e. before they reach memory.

Corrected model: TSO 2

Internal $\xrightarrow{rf}$ $(\xrightarrow{rfi})$ does not create order, external $\xrightarrow{rf}$ $(\xrightarrow{rfe})$ does:

let com-hb = rfe | fr | co #rfi not in hb  
acyclic ppo | com-hb | mfence

The new hb is no longer cyclic:

(Also consider that $a \xrightarrow{po} c$ and $d \xrightarrow{po} f$ are non-global.)
A new check: **uniproc**

We add a specific **uniproc** check to rule out coherence violations:

\[
\text{Irreflexive } \left(\text{po-loc}; \text{com}\right)
\]

Where \(\text{po-loc} \rightarrow\) is \(\text{po}\rightarrow\) between accesses to the same memory location.

let complus = rf | fr | co | (co;rf) | (fr;rf)
irreflexive (po-loc; complus) as uniproc

... In the TSO case we can “optimise”:

irreflexive rf;RW(po-loc)
irreflexive fr;WR(po-loc)

because the other coherence violations are rejected by the HB check.

---

**A word on uniproc**


**Definition (Uniproc 1)**

\[
\text{Acyclic } \left(\text{po-loc} \cup \text{com}\right)
\]

\[
\text{with } \text{com} = \text{rf} \cup \text{co} \cup \text{fr}.
\]

From cycle analysis, we have the more attractive definition (since relying on local action of the core and on the existence of coherence orders):

**Definition (Uniproc 2)**

\[
\text{Irreflexive } \left(\text{po-loc}; \text{com}\right)
\]

Definitions are equivalent.

---

**Our final TSO model**

TS03

let comhat = rf | fr | co | (co;rf) | (fr;rf)
irreflexive (po-loc; comhat) as uniproc

let ppo = (R*M | W*W) & po \# (W*R) & po absent
let com-hb = rfe | fr | co \# rfi absent
acyclic ppo | mfence | com-hb as hb

**Notice:** There are two checks... The axiomatic frameworks defines *principles* that the operational model/hardware implement.

For instead, we do not explain how **uniproc** is implemented. Instead, we specify admissible behaviours.

---

**Equivalence of uniproc definitions**

Uniproc 1 \(\Rightarrow\) Uniproc 2 is obvious, as \(\text{po-loc}; \text{com}\rightarrow\) is included in \(\left(\text{po-loc} \cup \text{com}\right)^+\) (since \(\text{com}\rightarrow\) = \((\text{com}\rightarrow\)^+).

Conversely, we use the “Identical locations” lemma.

Consider a cycle in \(\text{po-loc} \cup \text{com}\rightarrow\), s.t. for all \(e_1 \text{po-loc} \rightarrow e_2\) steps we do not have \(e_2 \text{com}\rightarrow\rightarrow e_1\). Then, for a given \(e_1 \text{po-loc} \rightarrow e_2\) step:

- Either, \(r_1 \text{po-loc} \rightarrow r_2\), with \(w \text{rf}\rightarrow r_1\) and \(w \text{rf}\rightarrow r_2\). We short-circuit the \(\text{po-loc}\rightarrow\) step, replacing \(w \text{rf}\rightarrow r_1 \text{po-loc} \rightarrow r_2\) by \(w \text{rf}\rightarrow r_2\).
- Or, \(e_1 \text{com}\rightarrow\rightarrow e_2\). We replace the \(\text{po-loc}\rightarrow\) step by \(\text{com}\rightarrow\) steps.

As a result we have a cycle in \(\text{com}\rightarrow\), which is impossible.
From TSO to x86-TSO: locked instructions

Those instructions perform a load then a store to the same location: they generate an atomic pair \( r \rightarrow w \). Additionally, \( r \) and \( w \) are tagged “atomic”.

**Example:** \texttt{xchg1 \( r, x \)}.

We further enforce:

- **Writes** \( w' \) to the location are either before the pair or after it:
  \[
  \left( r \xrightarrow{\text{rmw}} w \right) \implies \left( w' \xrightarrow{\text{rf}} r \lor w' \xrightarrow{\text{co}} w \right)
  \]

  Or more concisely, we forbid \( r \xrightarrow{\text{fr}} w' \xrightarrow{\text{co}} w \), that is no \( w' \) in-between.
  \[
  \left( r \xrightarrow{\text{rmw}} \cap \left( \xrightarrow{\text{fr}}; \xrightarrow{\text{co}} \right) \right) = \emptyset
  \]

- “Fence semantics”: locked instructions act as fences.

---

**ATOM check**

The **ATOM check** forbids this execution:

<table>
<thead>
<tr>
<th>( T_0 )</th>
<th>( T_1 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( r \leftarrow 1 )</td>
<td>( r \leftarrow 1 )</td>
</tr>
<tr>
<td>( (a/b) r \leftarrow x )</td>
<td>( (d/e) r \leftarrow y )</td>
</tr>
<tr>
<td>( (c) r0 \leftarrow y )</td>
<td>( (f) r1 \leftarrow x )</td>
</tr>
</tbody>
</table>

Observed? \( r=0; y=2 \)

---

**Implied fences**

Implied fences forbid this execution

**x86-TSO model for herd**

Predefined sets: \( W, R, M \) (any memory event), \( A \) (“atomic” memory event).

\[
(*) \text{ Uniproc } \ast
\]

let \( \text{comhat} = \text{rf} \lor \text{fr} \lor \text{co} \lor (\text{co};\text{rf}) \lor (\text{fr};\text{rf}) \lor (\text{rf}|\text{fr}|\text{co})+ \)

irreflexive \( \text{po} \); \( \text{comhat} \) as uniproc

\[
(*) \text{ Atomic pairs } \ast
\]

empty \( \text{rmw} \) & (\text{fre};\text{coe}) as atom

\[
(*) \text{ Implied fences (restricted to WR pairs) } \ast
\]

let \( \text{poWR} = (\ast W \ast R) \& \text{po} \)

let \( \text{implied} = (\ast M \ast A \lor A \ast M) \& \text{poWR} \)

\[
(*) \text{ Happens-before } \ast
\]

let \( \text{ppo} = (\ast R \ast M \lor W \ast W) \& \text{po} \lor \text{ppoWR} \)

\[
\text{let } \text{com-hb} = \text{rfe} \lor \text{fr} \lor \text{co} \lor \text{rfe};\text{fr};\text{co}+ \]

acyclic \( \text{ppo} \) | \( \text{mfence} \) | \( \text{implied} \) | \( \text{com-hb} \) as \( \text{hb} \)
Alternative formulation, or constrained domains and codomains

Given set $S$, $[S]$ is identity on $S$.
As a consequence, $[S_1]; [S_2]$ and $r \&(S_1 \ast S_2)$ are equal.

Then, for instance, we may reformulate TSO preserved program order as:

```plaintext
(* let ppo = (R*M|W*W) & po *)
let ppo = [R];po;[M] | [W];po;[W]
...```

A relaxed shared memory computer

More or less visible to user code:

- **Cores:**
  - Out of order execution
  - Branch speculation
  - Write buffers
- **Memory**
  - Physically distributed
  - Caches

Part 4.

Axiomatic ARM/Power

Situation of (our) ARM/Power models

- **Architecture public reference** Informal, cannot clearly explain how fences restore SC for instance.
- **Operational model:** (PLDI’11) more precise, developped with IBM experts. It is quite complex, and the simulator is very slow.
- **Multi-event axiomatic model:** (CAV’12) more precise (equivalent to PLDI’11), uses several events per access.
- **Single-event axiomatic model:** (TOPLAS’14) ARMv7 (ARM) and Power (PPC), more precise (proved to be more relaxed than PLDI’11, experimentally equivalent). A more simple axiomatic model.
- **ARMv8 (AArch64), official model, endorsed by ARM Ltd.**

Joint work with (in order of appearance) Jade Alglave, Susmit Sarkar, Peter Sewell, Derek Williams, Kayvan Memarian, Scott Owens, Mark Batty, Sela Mador-Haim, Rajeev Alur, Milo M. K. Martin and Michael Tautschnig.
Some issues for ARM/Power

- No simple preserved-program-order. More precisely, \( \text{ppo} \) will now account for core constraints, such as dependencies.
- Communication relations alone do not define happen-before steps.
- A variety of memory fences: lightweight (Power lwsync) and full (Power sync).

Two-threads SC violation for ARM

Generating tests is as simple as:
\[
% \text{diy } -\text{conf} \ 2\text{.conf} \ -\text{arch} \ \text{ARM}
\]
With the same configuration file 2.conf as for X86. Then, compile (in two steps, generate C locally, compile it on target machine), run and...

Observation R Sometimes 5722 1994278
Observation MP Sometimes 17439 1982561
Observation S Sometimes 7270 1992730
Observation SB Sometimes 9788 1990212
Observation LB Sometimes 4782 1995218
All Non-SC behaviours observed!

No hope to define \( \text{ppo} \) as simply as for TSO.

An experiment on ARM/Power

Consider test MP:

<table>
<thead>
<tr>
<th>Time</th>
<th>r0</th>
<th>r1</th>
</tr>
</thead>
<tbody>
<tr>
<td>T0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>T1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

\( \text{a: } \text{Wy}=1 \quad \text{c: } \text{Ry}=1 \quad \text{b: } \text{Wy}=1 \quad \text{d: } \text{Rx}=0 \)

We know that the test is Ok (observed, valid) on ARM/Power, what does it take (amongst fences, dependencies,) to make the test No (unobserved, invalid)?

- Fences: dsb, dmb, isb (ARM); sync, lwsync, isync (Power).
- Dependencies: address, data, control, control+isb/isync.

Dependencies (Power)

Address dependency:
\[
\begin{align*}
\text{r1} &\leftarrow \text{x} & \text{lzw} \ r1,0(\text{r8}) &\quad \text{r8 contains the address of 'x'} \\
\text{r2} &\leftarrow \text{t} [\text{r1}] & \text{slwi} \ r7, r1, 2 &\quad \text{sizeof(int) = 4} \\
\text{lwzx} \ r2, \text{r7}, \text{r9} &\quad \text{r9 contains the address of 't'}
\end{align*}
\]

Data dependency:
\[
\begin{align*}
\text{r1} &\leftarrow \text{x} & \text{lzw} \ r1,0(\text{r8}) &\quad \text{r8 contains the address of 'x'} \\
\text{y} &\leftarrow \text{r1}+1 & \text{addi} \ r2, r1, 1 & \text{stw} \ r2,0(\text{r9}) &\quad \text{r9 contains the address of 'y'}
\end{align*}
\]

Control dependency: (+isync)
\[
\begin{align*}
\text{r1} &\leftarrow \text{x} & \text{lzw} \ r1,0(\text{r8}) & \text{cmpwi} \ r1, 0 \\
\text{if } r1=0 &\quad \text{bne} \ L1 & \text{(isync)} \\
\text{(isync)} &\quad \text{li} \ r2, 1 & \text{stw} \ r2,0(\text{r9}) \\
\text{L1} &\end{align*}
\]
Generating tests (ARM), yet another tool: diycross

Generating tests with diycross (demo in demo/diycross):

```
% diycross -arch ARM
PodWW,DMBdWW,DSBdWW,ISBdWW
Rfe
Fre
Generator produced 28 tests
```

▶ One generates MP as diyone PodWW Rfe PodRR Fre
▶ diycross \( r_1 \cdots r_{N_1} \cdots r_{N_M} \cdot r_{M_1} \cdots r_{M_M} \) generates the \( N_1 \times \cdots \times N_M \) cycles \( r_1 \cdots r_{N_1} \cdots r_{N_M} \) by cross-producing the given edge list arguments.

This generates some variations in the MP family.

We then compile and run, and...

---

**Optimal fencing/dependencies for MP**

---

**Some observations**

In the previous slide we considered increasing power (and cost):

```
addr < lwsync < sync
```

Then:

- Dependencies (address) are sufficient to restore order from reads to writes and reads in two-threads examples (but...)
- Fences restore order from writes to write and reads.
- Full fence (sync) is required from write to read.
- When to use the lightweight fence between writes is complex:
  
  \( 2+2W+lwsyncs \) vs. \( R+lwsync+sync \).

---

**Optimal fencing for the 6 two-threads tests (Power)**

---

**Optimal fencing for the 6 two-threads tests (Power)**

---
Dependencies are enough

<table>
<thead>
<tr>
<th>CAUSAL</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_0$</td>
<td>$T_1$</td>
</tr>
<tr>
<td>(a) $r_0 \leftarrow x$</td>
<td>(c) $r_1 \leftarrow y$</td>
</tr>
<tr>
<td>(b) $y \leftarrow r_0$</td>
<td>(d) $x \leftarrow r_1$</td>
</tr>
</tbody>
</table>

Observed? $r_0=42$; $r_1=42$

a: $Rx=42$  c: $Ry=42$
b: $Wy=42$  d: $Wx=42$

LB+datas

Of course we never observe this behaviour (values out of thin air) and any (hardware) model should forbid it.

**Happens-before** If we order: (1) stores: the point in time when the value is made available to other threads (2) loads: the point when the value is read by core.

Dependencies from reads not always enough!

Consider test **WRC+data+addr**:

<table>
<thead>
<tr>
<th>WRC+data+addr</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_0$</td>
<td>$T_1$</td>
</tr>
<tr>
<td>(a) $x[0] \leftarrow 1$</td>
<td>(b) $r_0 \leftarrow x$</td>
</tr>
<tr>
<td>(c) $y \leftarrow r_0$</td>
<td>(e) $t \leftarrow r_1$</td>
</tr>
</tbody>
</table>

Observed? $r_0=1$; $r_2=0$

a: $Wx[0]=1$  c: $Wx[0]=1$
b: $Rx[0]=1$  d: $Wx[0]=1$
d: $Ry[0]=1$
a: $Ry[0]=1$

c: $Rx[0]=0$

d: $Rx[0]=0$

e: $Rx[0]=0$

WRC+data+addr

Behaviour is legal on Power 6,7 (observed) and ARMv7 (non observed).

Stores are not “multi-copy atomic”: $T_0$ and $T_1$ share a private buffer/cache/memory (e.g. a cache in SMT context). $T_2$ “does not see” the store by $T_0$, when $T_1$ does.

Restoring SC for **WRC**

Use a lightweight fence on $T_1$:

<table>
<thead>
<tr>
<th>T0</th>
<th>T1</th>
<th>T2</th>
</tr>
</thead>
<tbody>
<tr>
<td>a: $Wx=1$</td>
<td>rf</td>
<td>b: $Rx=1$</td>
</tr>
<tr>
<td></td>
<td>lwsync</td>
<td>rf</td>
</tr>
<tr>
<td>c: $Wy=1$</td>
<td>rf</td>
<td>d: $Ry=1$</td>
</tr>
</tbody>
</table>

WRC+lwsync+addr

Observation: The fence orders the writes a (by $T_0$) and c (by $T_1$) for any observer (here $T_2$). Similar to more simple **MP**

<table>
<thead>
<tr>
<th>T0</th>
<th>T1</th>
<th>T2</th>
</tr>
</thead>
<tbody>
<tr>
<td>a: $Wx=1$</td>
<td>lwsync</td>
<td>rf</td>
</tr>
<tr>
<td></td>
<td>rf</td>
<td>b: $Rx=1$</td>
</tr>
<tr>
<td>c: $Wy=1$</td>
<td>laddr</td>
<td>rf</td>
</tr>
</tbody>
</table>

MP+lwsync+addr

Another, symmetric, case of insufficient dependencies

Consider test **IRIW+addrs**:

<table>
<thead>
<tr>
<th>IRIW+addrs</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_0$</td>
<td>$T_1$</td>
</tr>
<tr>
<td>(a) $x[0] \leftarrow 1$</td>
<td>(b) $r_0 \leftarrow x[0]$</td>
</tr>
<tr>
<td>(c) $r_1 \leftarrow y[t]$</td>
<td>(f) $r_3 \leftarrow x[t]$</td>
</tr>
</tbody>
</table>

Observed? $r_0=1$; $r_1=1$; $r_2=1$; $r_3=0$

a: $Wx[0]=1$  c: $Wx[0]=1$
b: $Rx[0]=1$  d: $Wx[0]=1$
d: $Ry[0]=1$
a: $Ry[0]=1$

c: $Rx[0]=0$

d: $Rx[0]=0$

IRIW+addrs

Behaviour observed on Power (not on ARM, but documentation allows it).

Stores are not “multi-copy atomic”: $T_0$ and $T_1$ have a private buffer/cache/memory, $T_2$ and $T_3$ also have one.
Restoring SC for IRIW

Use a full fence on $T_1$ and $T_2$:

$\begin{array}{cccc}
T_0 & T_1 & & T_2 & T_3 \\
\text{a: Wx=1} & \text{rf} & \text{sync} & \text{rf} & \text{sync} \\
\text{b: Rx=1} & & & & \\
\text{c: Ry=0} & \text{fr} & & \\
\text{d: Wy=1} & & & & \\
\text{e: Ry=1} & & & & \\
\text{f: Rx=0} & & & & \\
\end{array}$

IRIW+syncs

Propagation: Full fences order all communications.

A model in four checks (TOPLAS’14)

**UNIPROC**
acyclic poloc | com as uniproc

**NO-THIN-AIR**
let fence = strong | light
let hb = ppo | fence | rfe
acyclic hb as no-thin-air

**OBSERVATION** We now define the effect of fences (any fence) for ordering writes:

$\text{let propbase} = (((W*W) & fence)|(rfe; ((R*W) & fence)));hb*$

irreflexive fre;propbase as observation

**PROPAGATION** Strong fences wait for all communications. Simple formulation:

let com = rf|fr|co
acyclic com|strong as propagation

In actual model, a more strict condition:

let prop = (W*W)&propbase|((com*;propbase*;strong;hb*)
acyclic co | prop as propagation

Relation summary

Communication relations:

- Read-from: $w \xrightarrow{fr} r$, with $\text{loc}(w) = \text{loc}(r), \text{val}(w) = \text{val}(r)$.
- Coherence: $w \xrightarrow{co} w'$, with $\text{loc}(w) = \text{loc}(w') = x$. Total order for given $x$: hence “coherence orders”.
- We deduce from-read: $r \xrightarrow{fr} w$, i.e. $w' \xrightarrow{fr} r$ and $w' \xrightarrow{co} w$.
- We distinguish internal (same proc, $\text{rfi} \rightarrow \text{coi} \rightarrow \text{fri} \rightarrow$) and external (different pros, $\text{rfe} \rightarrow \text{coe} \rightarrow \text{fre} \rightarrow$) communications.

“Execution” relations

- Program order: $e_1 \xrightarrow{po} e_2$, with $\text{proc}(e_1) = \text{proc}(e_2)$.
- Same location program order: $e_1 \xrightarrow{po-loc} e_2$.
- Preserved program order: $e_1 \xrightarrow{ppo} e_2$, with $\text{ppo} \rightarrow \subseteq \text{po} \rightarrow$. Computed from other relations, includes (effective) dependencies (control dependency from read to read is not effective).
- Fences: effective strong and lightweight fences in between events $\xrightarrow{strong}$ and $\xrightarrow{light}$. Effective means that for instance $w \xrightarrow{lwsync} r$ does not implies $w \xrightarrow{light} r$.

ARM/Power preserved program order

Rather complex, results from a two events per access analysis (cf. CAV’12).

(* Utilities *)
let dd = addr | data
let rdw = po-loc & (fre;rf)
let detour = po-loc & (coe; rfe)
let addrpo = addr;po

(* Initial value *)
let ci0 = ctrlisync | detour
let ii0 = dd | rfi | rdw
let cc0 = dd | po-loc | ctrl | addrpo
let ic0 = 0

(* Fixpoint from i -> c in instructions and transitivity *)
let rec ci = ci0 | (ci;ii) | (cc;ci)
and ii = i0 | ci | (ic;ci) | (ii;ii)
and cc = cc0 | ci | (ci;ic) | (cc;cc)
and ic = ic0 | ii | cc | (ic;cc) | (ii ; ic)

let ppo = [R]; ic; [W] | [R]; ii; [R]
Can be limited to dependencies...
ARMv8 is an “other multicopy atomic” architecture.

That is, writes are “performed” for all participants, as soon as “performed” for one (external) participant.

As regards tests, this means that, say WRC+data+addr and IRIW+addr are forbidden (but SB+rfi-addr, cf. slide 57, is still allowed).

From the axiomatic point of view, rfe (as well as fr and co) is part of happens-before. And the CAT model is simplified.

In effect, no-thin-air, observation and propagation can be performed by one single check, here called “EXTERNAL”.

A few details

Armv8 features load-acquire instructions — two of them, Acquire (LDAR) and AcquirePC (LDAPR), events A and Q; and store-release instructions — STLR, events L.

(* Barrier-ordered-before *)
let bob = ... # Fences left out
| [A | Q]; po   # Acquire
| po; [L]     # Release
| [L]; po; [A] #

let lob = ... | bob | ...

let ob = rfe | fre | coe | ... | lob | ...

Those rules, plus external communication being part of ordered-before entails that using load-acquire and store-releases restores SC.

Part 5.

Axiomatic C11
The C11, memory model, quick starter

C11 features "atomic" scalar types atomic_int, etc. and "atomic" operations atomic_store_explicit(p, v, m), atomic_load_explicit(p, m) (and more...).

It also feature fences atomic_thread_fence(m).

Where m is a "memory-order", relaxed, acquire, release, sequential consistent (and consume, neglected), with annoyingly long names memory_order_relaxed, ..., memory_order_seq_cst.

In CAT memory-order specifications result in sets of events RLX, ACQ, ..., SC. Those events can be reads or writes (sets R and W) but also fences (set F).

(Repaired) C11 model. happens-before

The happens-before, hb relation is build from sb (sequenced-before, C-style program-order). and sw (synchronize-with). Notice that this sequence is similar to critical sections ordering: Lock is akin to load-acquire, UnLock to store-release.

RC11 happens-before, the full story

We have release-sequence, rs:

let RLX-OR-MORE = RLX|REL|ACQ_REL|ACQ|SC
let sb-loc = sb & loc
let rs = [W]; sb-loc?; [W & RLX-OR-MORE];(rf;rmw)*

Notice that rs includes [W & REL], the most simple "release sequence".

Then, full synchronise-with:

let REL-OR-MORE = REL | ACQ_REL | SC
and ACQ-OR-MORE = ACQ | ACQ_REL | SC
let sw = [REL-OR-MORE]; ([F]; sb)?; rs; rf;
[R & RLX-OR-MORE]; (sb; [F])?; [ACQ-OR-MORE]
let hb = (sb | sw)
RC11, uniproc and propagation

let eco = (rf|fr|co)+ // Our old friend

irreflexive hb; eco? as coherence
Interestingly, “coherence” above regroups both UNIPROC (sb included in hb) and some generalised OBSERVATION (communication vs. hb)

Out of thin-air values cannot be neglected
▶ If any value can pop-up at any time no program proof is possible.
▶ Allowing LB+datas over non-atomics (for instance) hinders the DRF theorem.
▶ Out-of-thin-air values are not precisely defined, partly because dependencies are difficult to define in a (optimised) programming language.

Restoring SC: the big deal of RC11
For SC atomics:

RC11 radical stance agains out-of-thin-air
Forbid any “LB” shape.

acyclic sb | rfe as no-thin-air
To be compared with machine level NO-THIN-AIR

acyclic ppo | fence | rfe as no-thin-air
As a result, “causality” cycles are radically excluded.

Still in discussion, because such a solution entails a (light in our opinion) runtime penalty.

At present, alternative solutions are complex, roughly in operational semantics terms: they rely on forging values for reads (promises), and then checking that promises are fulfilled by any possible reduction in any context.

int r0 = atomic_load_explicit(x, memory_order_relaxed) ;
int r1 = 0 ;
if (r0 == 42) { r1 = 42; } else { r1 = 42; }
atomic_store_explicit(y, r1, memory_order_relaxed) ;

int r2 = atomic_load_explicit(y, memory_order_relaxed) ;
atomic_store_explicit(x, r2, memory_order_relaxed) ;
Allow? (include sophisticated control dependencies definition in hb)
Forbid? (hinders optimisation?)

Acyclicity of pscf entails “simple” strong fence SC-preserving condition
acyclic [F]; hb; eco ; sb; [F] # or acyclic eco; sb; [F]; hb

Relation scb always includes a sb step in case included in hb\loc.
This is weaker than simply including hb in scb. But it provides steps compilation schemes that use strong fences for implementing SC atomics.

Fence semantics significantly strengthened w.r.t. previous C11 formulations.
How good are our models?

Are they sound?

- Proofs of equivalence or at least of axiomatic models being weaker than operational ones.
- Proof of compilation correctness (from RC11 to...).
- Experiments
  - Soundness w.r.t. hardware (ARMv7 being a bit problematic because of acknowledged read-after-read hazard).
  - Experimental equivalence with our previous models.

Above all:

- Vendor approval (ARM Ltd. for ARMv8).
- Comitee acceptance (almost for RC11).

In any case:

- Simulation is fast.
- The existence of four checks UNIPROC, HB OBSERVATION and PROPAGATION stand on firm bases.
- The semantics of strong fences also does.
- The model and simulator (i.e. herd) are flexible, one easily change a few relations (e.g. \( \text{ppo}\), or the semantics of weak fences).

### Bug or feature?

The following execution:

\[
\begin{align*}
\text{a: } & Wz=1 \\
\text{b: } & Ry=0 \\
\text{c: } & Rz=2 \\
\text{d: } & Rz=1 \\
\text{e: } & Wz=2
\end{align*}
\]

is observed on all (tested) ARMv7 machines. It features a CoRR-style coherence violation (i.e. \( \text{ppo} \) contradicts \( \text{fr} \)). Notice: CoRR is not observed directly.

- Definitively a hardware anomaly.
- Not observed on ARMv8.

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Some valuable readings you now have been introduced to

